CLAIMS

What is claimed is:

1. A transceiver circuit capable of transferring data at one or more transfer rates, the transceiver circuit comprising:

one or more state machines having one or more tone phases in which determination of the maximum transfer rate for one or more channels and one or more connections with one or more remote devices is carried out through exchange of one or more tone signals with at least one of the remote device or devices, and one or more data transfer phases in which data transfer is carried out at one or more frequencies higher than that of at least one of the tone signal or signals;

one or more error detection circuits detecting one or more errors in one or more receive signals; and

one or more data transfer phase transition suppressor circuits;

wherein, in the event that at least one of the error detection circuit or circuits detects at least one of the error or errors within at least one of the receive signal or signals during at least one of the data transfer phase or phases, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases, and after at least one of such transition or transitions has occurred, at least one of the data transfer phase transition suppressor circuit or circuits carries out control so as to prevent transition back to at least one of the data transfer phase or phases.

2. A transceiver circuit according to claim 1 further comprising:

one or more timers; and

one or more error counters;

wherein, only in the event that one or more numbers of errors occurring within one or more fixed times as detected by at least one of the error detection circuit or circuits, at least one of the timer or timers, and at least one of the error counter or counters during at least one of the data transfer phase or phases is greater than at least one preestablished value, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases, and after at least one of such transition or transitions has occurred, at least one of the data transfer phase transition suppressor

circuit or circuits carries out control so as to prevent transition back to at least one of the data transfer phase or phases.

3. A transceiver circuit according to claim 1 further comprising:

one or more transfer rate comparison circuits comparing the minimum transfer rate of which the transceiver circuit is capable and one or more transfer rates employed during at least one of the data transfer phase or phases;

wherein, only in the event that at least one of the error detection circuit or circuits detects at least one of the error or errors and at least one of the transition or transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases when at least one result of at least one comparison made by at least one of the transfer rate comparison circuit or circuits is that at least one of the transfer rate or rates employed during at least one of the data transfer phase or phases is identical to the minimum transfer rate or rates of which the transceiver circuit is capable, at least one of the data transfer phase transition suppressor circuit or circuits carries out control so as to prevent transition back to at least one of the data transfer phase or phases.

4. A transceiver circuit capable of transferring data at one or more transfer rates, the transceiver circuit comprising:

one or more state machines having one or more tone phases in which one or more connections with one or more remote devices are established through exchange of one or more tone signals with at least one of the remote device or devices, one or more speed negotiation phases in which determination of the maximum transfer rate permitted by one or more channels is carried out through mutual notification of one or more transfer rates of which the local device is capable, this notification being actually carried out at at least one of such transfer rate or rates, and one or more data transfer phases in which data transfer is carried out at at least one of the transfer rate or rates determined at at least one of the speed negotiation phase or phases;

one or more error detection circuits detecting one or more errors in one or more receive signals; and

one or more speed negotiation phase transition suppressor circuits;

wherein, in the event that at least one of the error detection circuit or circuits detects at least one of the error or errors within at least one of the receive signal or signals during

at least one of the data transfer phase or phases, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases, and after at least one of such transition or transitions has occurred, at least one of the speed negotiation phase transition suppressor circuit or circuits carries out control so as to prevent transition to at least one of the speed negotiation phase or phases.

5. A transceiver circuit capable of transferring data at one or more transfer rates, the transceiver circuit comprising:

one or more state machines having one or more tone phases in which one or more connections with one or more remote devices are established through exchange of one or more tone signals with at least one of the remote device or devices, one or more speed negotiation phases in which determination of one or more maximum transfer rates permitted by one or more channels is carried out through mutual notification of one or more transfer rates of which the local device is capable, this notification being actually carried out at at least one of such transfer rate or rates, and one or more data transfer phases in which data transfer is carried out at at least one of the transfer rate or rates determined at at least one of the speed negotiation phase or phases;

one or more error detection circuits detecting one or more errors in one or more receive signals; and

one or more speed negotiation phase transition suppressor circuits;

wherein, in the event that at least one of the error detection circuit or circuits detects at least one of the error or errors within at least one of the receive signal or signals during at least one of the speed negotiation phase or phases, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases, and after at least one of such transition or transitions has occurred, at least one of the speed negotiation phase transition suppressor circuit or circuits carries out control so as to prevent transition to at least one of the speed negotiation phase or phases.

6. A transceiver circuit according to claim 4 or 5 further comprising:

one or more timers; and

one or more error counters;

wherein, only in the event that one or more numbers of errors occurring within one or more fixed times as detected by at least one of the error detection circuit or circuits, at

least one of the timer or timers, and at least one of the error counter or counters is greater than at least one preestablished value, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases, and after at least one of such transition or transitions has occurred, at least one of the state machine phase transition suppressor circuit or circuits carries out control so as to prevent transition to at least one of the speed negotiation phase or phases.

7. A transceiver circuit according to claim 4 or 5 further comprising:

one or more transfer rate comparison circuits comparing minimum transfer rate of which the transceiver circuit is capable and one or more transfer rates employed during at least one of the data transfer phase or phases;

wherein, only in the event that at least one of the error detection circuit or circuits detects at least one of the error or errors and at least one of the transition or transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases when at least one result of at least one comparison made by at least one of the transfer rate comparison circuit or circuits is that at least one of the transfer rate or rates employed during at least one of the data transfer phase or phases is identical to at least one of the minimum transfer rate or rates of which the transceiver circuit is capable, at least one of the speed negotiation phase transition suppressor circuit or circuits carries out control so as to prevent transition to at least one of the speed negotiation phase or phases.

8. A transceiver circuit according to claim 4 or 5 further comprising:

one or more counters; and

one or more timers;

wherein the transceiver circuit is OP i.LINK-compliant;

wherein at least one of the counter or counters counts one or more numbers of transitions from at least one of the tone phase or phases to at least one of the speed negotiation phase or phases; and

wherein, in the event that at least one of the number or numbers of transitions as counted by at least one of the counter or counters reaches at least one preestablished value within at least one fixed time, it being determined that channel quality is poor, at least one of the speed negotiation phase transition suppressor circuit or circuits carries

out control so as to prevent transition to at least one of the speed negotiation phase or phases.

9. A transceiver circuit according to claim 2, 3, 6, 7, or 8 wherein:

one or more tone signal transmit select circuits are employed as at least one of the data transfer phase transition suppressor circuit or circuits or speed negotiation phase transition suppressor circuit or circuits; and

in the event that at least one of the error detection circuit or circuits determines that channel quality is poor and one or more transitions is made from at least one of the data transfer phase or phases to at least one of the speed negotiation phase or phases, at least one of the tone signal transmit select circuit or circuits carries out control so as to prevent transmission of one or more tone signals.

10. A transceiver circuit according to claim 9 further comprising:

one or more receive signal detection circuits; and

one or more timers;

wherein, in the event that at least one of the receive signal detection circuit or circuits and at least one of the timer or timers establish during at least one of the tone phase or phases that at least one receive signal, being absent for not less than at least one fixed time, has been completely disconnected, at least one of the tone signal transmit select circuit or circuits reinitiates transmission of one or more tone signals.

11. A transceiver circuit according to claim 9 further comprising:

one or more cable connect detection circuits;

wherein, in the event that at least one of the cable connect detection circuit or circuits establishes during at least one of the tone phase or phases that one or more cables has been disconnected, at least one of the tone signal transmit select circuit or circuits reinitiates transmission of one or more tone signals after at least one of the cable or cables has been reconnected.

12. A transceiver circuit according to claim 2, 3, 6, 7, or 8 wherein:

one or more transmitter power supply control circuits are employed as at least one of the data transfer phase transition suppressor circuit or circuits or speed negotiation phase transition suppressor circuit or circuits; and

in the event that at least one of the error detection circuit or circuits determines that

channel quality is poor, one or more transitions is made to at least one of the tone phase or phases, and after at least one of such transition or transitions has occurred, at least one of the transmitter power supply control circuit or circuits causes at least one power supply of at least one transmitter to be turned OFF.

13. A transceiver circuit according to claim 12 further comprising:

one or more receive signal detection circuits; and

one or more timers;

wherein, in the event that at least one of the receive signal detection circuit or circuits and at least one of the timer or timers establish during at least one of the tone phase or phases that at least one receive signal, being absent for not less than at least one fixed time, has been completely disconnected, at least one of the transmitter power supply control circuit or circuits causes at least one power supply of at least one transmitter to be turned ON.

14. A transceiver circuit according to claim 12 further comprising:

one or more cable connect detection circuits;

wherein, in the event that at least one of the cable connect detection circuit or circuits establishes during at least one of the tone phase or phases that one or more cables has been disconnected, at least one of the transmitter power supply control circuit or circuits causes at least one power supply of at least one transmitter to be turned ON after at least one of the cable or cables has been reconnected.

15. A transceiver circuit according to claim 6, 7, or 8 wherein:

the transceiver circuit is OP i.LINK-compliant;

one or more TPBIAS mask circuits provided at one or more PORT locations is or are employed as at least one of the speed negotiation phase transition suppressor circuit or circuits; and

in the event that at least one of the error detection circuit or circuits determines that channel quality is poor, one or more transitions is made to at least one of the tone phase or phases, and thereafter at least one of the TPBIAS mask circuit or circuits masks one or more TPBIAS signals from at least one PHY carries out control so as to prevent transmission of one or more long tones and/or one or more continuous signals even if at least one TPBIAS is active.

16. A transceiver circuit according to claim 15 further comprising:

one or more receive signal detection circuits; and

one or more timers;

wherein, in the event that at least one of the receive signal detection circuit or circuits and at least one of the timer or timers establish during at least one of the tone phase or phases that at least one receive signal, being absent for not less than at least one fixed time following transmission of one or more tone signals by one or more local transmit circuits, has been completely disconnected, at least one of the mask or masks applied to at least one of the TPBIAS signal or signals by at least one of the TPBIAS mask circuit or circuits is removed, causing one or more long tone signals and/or one or more continuous signals to be transmitted when at least one TPBIAS is active.

17. A transceiver circuit according to claim 15 further comprising:

one or more cable connect detection circuits;

wherein, in the event that at least one of the cable connect detection circuit or circuits establishes during at least one of the tone phase or phases that one or more cables has been disconnected, at least one of the mask or masks applied to at least one of the TPBIAS signal or signals by at least one of the TPBIAS mask circuit or circuits is removed after at least one of the cable or cables has been reconnected, causing one or more long tone signals and/or one or more continuous signals to be transmitted when at least one TPBIAS is active.

18. A transceiver circuit according to claim 6, 7, or 8 wherein:

the transceiver circuit is OP i.LINK-compliant;

one or more TPBIAS suppressor circuits provided at one or more PHY locations is or are employed as at least one of the speed negotiation phase transition suppressor circuit or circuits; and

in the event that at least one of the error detection circuit or circuits determines that channel quality is poor, one or more transitions is made to at least one of the tone phase or phases, and thereafter, even if at least one TPBIAS is active within at least one of the PHY location or locations, at least one of the TPBIAS suppressor circuit or circuits carries out control so as to prevent at least one of the PORT location or locations from being notified of the fact that the at least one TPBIAS is active.

19. A transceiver circuit according to claim 18 further comprising:

one or more receive signal detection circuits; and

one or more timers;

wherein, in the event that at least one of the receive signal detection circuit or circuits and at least one of the timer or timers establish during at least one of the tone phase or phases that at least one receive signal, being absent for not less than at least one fixed time following transmission of one or more tone signals by one or more local transmit circuits, has been completely disconnected, at least one of the TPBIAS suppressor circuit or circuits causes at least one of the PORT location or locations to be notified of at least one value of at least one TPBIAS signal within at least one of the PHY location or locations.

20. A transceiver circuit according to claim 18 further comprising:

one or more cable connect detection circuits;

wherein, in the event that at least one of the cable connect detection circuit or circuits establishes during at least one of the tone phase or phases that one or more cables has been disconnected, at least one of the TPBIAS suppressor circuit or circuits, after at least one of the cable or cables has been reconnected, causes at least one of the PORT location or locations to be notified of at least one value of at least one TPBIAS signal within at least one of the PHY location or locations.

21. A transceiver circuit according to claim 6, 7, or 8 wherein:

the transceiver circuit is OP i.LINK-compliant;

one or more BIAS_DETECT suppressor circuits provided at one or more PORT locations is or are employed as at least one of the speed negotiation phase transition suppressor circuit or circuits; and

in the event that at least one of the error detection circuit or circuits determines that channel quality is poor, one or more transitions is made to at least one of the tone phase or phases, and thereafter, even if one or more long tones and/or one or more continuous signals is or are received from one or more remote devices by at least one of the PORT location or locations and at least one BIAS_DETECT is active, at least one of the BIAS_DETECT suppressor circuit or circuits carries out control so as to prevent at least

one of one PHY location or locations from being notified of the fact that the at least one BIAS_DETECT is active.

22. A transceiver circuit according to claim 21 further comprising:

one or more receive signal detection circuits; and

one or more timers;

wherein, in the event that at least one of the receive signal detection circuit or circuits and at least one of the timer or timers establish during at least one of the tone phase or phases that at least one receive signal, being absent for not less than at least one fixed time following transmission of one or more tone signals by one or more local transmit circuits, has been completely disconnected, at least one of the BIAS_DETECT suppressor circuit or circuits causes at least one of the PHY location or locations to be notified of at least one value of at least one BIAS_DETECT signal within at least one of the PORT location or locations.

23. A transceiver circuit according to claim 21 further comprising:

one or more cable connect detection circuits;

wherein, in the event that at least one of the cable connect detection circuit or circuits establishes during at least one of the tone phase or phases that one or more cables has been disconnected, at least one of the BIAS_DETECT suppressor circuit or circuits, after at least one of the cable or cables has been reconnected, causes at least one of the PHY location or locations to be notified of at least one value of at least one BIAS_DETECT signal within at least one of the PORT location or locations.

24. A transceiver circuit according to claim 6, 7, or 8 wherein:

the transceiver circuit is OP i.LINK-compliant;

one or more BIAS_DETECT mask circuits provided at one or more PHY locations is or are employed as at least one of the speed negotiation phase transition suppressor circuit or circuits; and

in the event that at least one of the error detection circuit or circuits determines that channel quality is poor, one or more transitions is made to at least one of the tone phase or phases, and thereafter, even if one or more BIAS_DETECT signals is active, masking by at least one of the BIAS_DETECT mask circuit or circuits of at least one BIAS_DETECT signal from at least one of the PORT location or locations carries out

control so as to prevent at least one of the PHY location or locations from being notified of the fact that the at least one BIAS_DETECT signal is active.

25. A transceiver circuit according to claim 24 further comprising:

one or more receive signal detection circuits; and

one or more timers;

wherein, in the event that at least one of the receive signal detection circuit or circuits and at least one of the timer or timers establish during at least one of the tone phase or phases that at least one receive signal, being absent for not less than at least one fixed time following transmission of one or more tone signals by one or more local transmit circuits, has been completely disconnected, at least one of the mask or masks applied to at least one of the BIAS_DETECT signal or signals by at least one of the BIAS_DETECT mask circuit or circuits is removed, causing at least one of the PHY location or locations to be notified of the fact that at least one BIAS_DETECT is active when the at least one BIAS_DETECT is active.

26. A transceiver circuit according to claim 24 further comprising:

one or more cable connect detection circuits;

wherein, in the event that at least one of the cable connect detection circuit or circuits establishes during at least one of the tone phase or phases that one or more cables has been disconnected, at least one of the mask or masks applied to at least one of the BIAS_DETECT signal or signals by at least one of the BIAS_DETECT mask circuit or circuits is removed after at least one of the cable or cables has been reconnected, causing at least one of the PHY location or locations to be notified of the fact that the at least one BIAS_DETECT is active when the at least one BIAS_DETECT is active.

27. A transceiver circuit according to claim 2, 3, 6, 7, or 8 wherein:

the transceiver circuit is IEEE 1394-compliant;

one or more suspend/disable control circuits provided at one or more PHY locations is or are employed as at least one of the speed negotiation phase transition suppressor circuit or circuits; and

in the event that at least one of the error detection circuit or circuits determines that channel quality is poor, at least one of the suspend/disable control circuit or circuits, during at least one of the tone phase or phases, causes at least one PORT at which at least

one error is or was detected to enter at least one suspended state and/or at least one disabled state.

28. A transceiver circuit according to claim 27 further comprising:

one or more receive signal detection circuits; and

one or more timers;

wherein, in the event that at least one of the receive signal detection circuit or circuits and at least one of the timer or timers establish during at least one of the tone phase or phases that at least one receive signal, being absent for not less than at least one fixed time following transmission of one or more tone signals by one or more local transmit circuits, has been completely disconnected, at least one of the suspend/disable control circuit or circuits causes termination of at least one suspended state and/or at least one disabled state.

29. A transceiver circuit according to claim 27 further comprising:

one or more cable connect detection circuits;

wherein, in the event that at least one of the cable connect detection circuit or circuits establishes during at least one of the tone phase or phases that one or more cables has been disconnected, at least one of the suspend/disable control circuit or circuits causes termination of at least one suspended state and/or at least one disabled state after at least one of the cable or cables has been reconnected.

30. A transceiver circuit according to claim 2, 3, 6, 7, or 8 wherein:

one or more wait states is or are present between at least one of the data transfer phase or phases and at least one of the tone phase or phases; and

in the event that at least one of the error detection circuit or circuits determines that channel quality is poor, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the wait state or states, and only if it is established during at least one of the wait state or states that at least one remote device has been completely disconnected therefrom is at least one transition made to at least one of the tone phase or phases.

31. A transceiver circuit according to claim 30 further comprising:

one or more receive signal detection circuits; and

one or more timers;

wherein, in the event that at least one of the receive signal detection circuit or circuits and at least one of the timer or timers establish during at least one of the tone phase or phases that at least one receive signal, being absent for not less than at least one fixed time following transmission of one or more tone signals by one or more local transmit circuits, has been completely disconnected, at least one transition is made from at least one of the wait state or states back to at least one of the tone phase or phases.

32. A transceiver circuit according to claim 30 further comprising:

one or more cable connect detection circuits;

wherein, in the event that at least one of the cable connect detection circuit or circuits establishes during at least one of the tone phase or phases that one or more cables has been disconnected, at least one transition is made from at least one of the wait state or states back to at least one of the tone phase or phases after at least one of the cable or cables has been connected.

33. A transceiver circuit capable of transferring data at a plurality of transfer rates, the transceiver circuit comprising:

one or more state machines having one or more tone phases in which one or more connections with one or more remote devices are established through exchange of one or more tone signals with at least one of the remote device or devices, one or more speed negotiation phases in which determination of the maximum transfer rate permitted by one or more channels is carried out through mutual notification of one or more transfer rates of which one or more local devices is capable, this notification being actually carried out at at least one of such transfer rate or rates, and one or more data transfer phases in which data transfer is carried out at at least one of the transfer rate or rates determined at at least one of the speed negotiation phase or phases;

one or more error detection circuits detecting one or more errors in one or more receive signals; and

one or more transfer rate comparison circuits comparing the minimum transfer rate of the transceiver circuit and one or more transfer rates employed during at least one of the data transfer phase or phases;

wherein, in the event that at least one of the error detection circuit or circuits detects at least one of the error or errors within at least one of the receive signal or signals during

at least one of the data transfer phase or phases when at least one result of at least one comparison made by at least one of the transfer rate comparison circuit or circuits is that at least one of the transfer rate or rates employed during at least one of the data transfer phase or phases is greater than the minimum transfer rate or rates of the transceiver circuit, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases, and thereafter, the maximum transfer rate of the transceiver circuit during at least one of the speed negotiation phase or phases is set so as to be at least one rate that is lower than at least one transfer rate employed during at least one of the data transfer phase or phases.

34. A transceiver circuit according to claim 33 further comprising:

one or more receive signal detection circuits; and

one or more timers;

wherein, in the event that at least one of the receive signal detection circuit or circuits and at least one of the timer or timers establish during at least one of the tone phase or phases that at least one receive signal, being absent for not less than at least one fixed time following transmission of one or more tone signals by one or more local transmit circuits, has been completely disconnected, the maximum transfer rate of the transceiver circuit during at least one of the speed negotiation phase or phases is returned to its original maximum transfer rate.

35. A transceiver circuit according to claim 33 further comprising:

one or more cable connect detection circuits;

wherein, in the event that at least one of the cable connect detection circuit or circuits establishes during at least one of the tone phase or phases that one or more cables has been disconnected, the maximum transfer rate of the transceiver circuit during at least one of the speed negotiation phase or phases is returned to its original maximum transfer rate after at least one of the cable or cables has been reconnected.

36. A transceiver circuit according to claim 10 or 13 wherein the at least one fixed time is not less than 132 ms.

37. A transceiver circuit according to claim 16, 19, 22, 25, 28, 31, or 34 wherein the at least one fixed time is not less than 64 ms and not more than 132 ms.

38. A transceiving method substantially effects manifestation of one or more transceiver circuits according to any one of claims 1 through 37.

39. A transceiver apparatus comprising:

one or more transceiver circuits substantially according to any one of claims 1 through 37; and

one or more external display apparatuses;

wherein, in the event that at least one of the error detection circuit or circuits determines that channel quality is poor during at least one of the data transfer phase or phases or speed negotiation phase or phases, and at least one of the transceiver circuit or circuits is in one or more suppressed states selected from among the group consisting of suppression with respect to transition to at least one of the data transfer phase or phases, suppression with respect to transition to at least one of the speed negotiation phase or phases, and suppression with respect to maximum transfer rate during at least one of the speed negotiation phase or phases, one or more users are notified of such fact by means of at least one of the external display apparatus or apparatuses.